



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,701	04/19/2000	Shigemasa Haruhiko	1248-0497P-SP	3009

7590 05/28/2003  
Birch Stewart Kolasch & Birch LLP  
PO Box 747  
Falls Church, VA 22040-0747

EXAMINER

PUENTE, EMERSON C

ART UNIT	PAPER NUMBER
----------	--------------

2184

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/552,701

Applicant(s)

HARUHIKO ET AL.

Examiner

Emerson C Puente

Art Unit

2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8,9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

1. Claims 1 and 3-14 have been examined.
2. This action is made **FINAL**.

### *Claim Objections*

3. Claim 9 is objected to because of the following informalities:

In regards to claim 9, the limitation set forth is disclosed in newly amended independent claim 8. Examiner recommends applicant to cancel claim 9.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6, 8-11, and 13 are rejected under 35 U.S.C. §102(b) as being clearly anticipated by Japanese Patent No. 01-223586 of Omichi et al. referred hereinafter "Omichi".

In regards to claim 1, Omichi discloses a microcomputer having a built-in nonvolatile memory including:

a communication circuit for receiving a test program for a nonvolatile memory for an external check system (see figure 1 and page 5) ; and

a RAM on which said test program is run (see item 5 figure 1 and page 9).

Art Unit: 2184

a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 3, Omichi discloses a microcomputer having a built-in nonvolatile memory including:

- a nonvolatile memory (see item 4 figure 1);

- a boot ROM (see item 4 figure 1);

- a RAM (see item 5 figure 1);

- a CPU for running a program stored in said boot ROM and RAM (see item 5 figure 1); and

a communication circuit for controlling a communication with a check system (see figure 1), said boot ROM having stored a control program for jobs of:

- receiving a test program for said nonvolatile memory from said check system to be stored in said RAM at a test command issued from said check system (see page 7 and 9);

- running said test program (see page 6); and

- sending a test result to said check system (see page 6)

In regards to claim 4, Omichi discloses a check system of a microcomputer having a built-in nonvolatile memory furnished with:

- at least one external communication device connected to said microcomputer in such a manner so as to allow a communication in a one-to-one correspondence. Omichi discloses the microcomputer is mounted to a reader/writer (or host computer) and exchanges data with the reader/writer (see page 6);

- each external communication device including,

- a storage device having a stored a test program for a built-in nonvolatile memory in said microcomputer. Omichi indicates the storage of the operations test program in the testing device (see page 8), and

a communication microcomputer for sending said test program to said microcomputer. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with microcomputer, enabling it to send said test program to said microcomputer.

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 6, Omichi discloses a check system of a microcomputer having a built-in nonvolatile memory furnished with an external communication device including:

a storage device having stored a test program for said microcomputer having a built-in nonvolatile memory . Omichi indicates the storage of the operations test program in the testing device (see page 8),

a communication control circuit for controlling a communication with said microcomputer. Omichi discloses sending of data blocks from the external device containing mode identification information to determine kind of processing, which constitutes controlling a communication with said microcomputer(see page 7).

a communication microcomputer for sending said test program to said microcomputer when checking the built-in nonvolatile memory therein. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with microcomputer, enabling it to send said test program to said microcomputer.

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 8, Omichi discloses the an IC card packing a microcomputer having a built-in nonvolatile memory including:

Art Unit: 2184

a communication circuit for receiving a test program for a nonvolatile memory for an external check system (see figure 1 and page 5) ; and

a RAM on which said test program is run (see item 5 figure 1 and page 9).

a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 9, Omichi discloses the IC card further including a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 10, Omichi discloses an IC card packing a computer having a built-in nonvolatile memory including:

a nonvolatile memory (see item 4 figure 1);

a boot ROM (see item 4 figure 1);

a RAM (see item 5 figure 1);

a CPU for running a program stored in said boot ROM and RAM (see item 5 figure 1); and

a communication circuit for controlling a communication with a check system (see figure 1),

said boot ROM having stored a control program for jobs of:

receiving a test program for said nonvolatile memory from said check system to be stored in said RAM at a test command issued from said check system (see page 7 and 9);

running said test program (see page 6); and

sending a test result to said check system (see page 6)

In regards to claim 11, Omichi discloses a check system of an IC card packing a microcomputer having a built-in nonvolatile memory furnished with:

at least one external communication device connected to said microcomputer packed in said IC card in such a manner so as to allow a communication in a one-to-one correspondence. Omichi discloses the IC card mounted to a reader/writer (or host computer) and exchanges data with the reader/writer (see page 6);

each external communication device including,

a storage device having a stored a test program for a built-in nonvolatile memory in said microcomputer. Omichi indicates the storage of the operations test program in the testing device (see page 8), and

a communication microcomputer for sending said test program to said IC card. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with IC card, enabling it to send said test program to said IC card.

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

In regards to claim 13, Omichi discloses a check system of an IC card packing a microcomputer having a built-in nonvolatile memory furnished with an external communication device including:

a storage device having stored a test program for a built-in nonvolatile memory in said microcomputer packed in said IC card. Omichi indicates the storage of the operations test program in the testing device (see page 8),

a communication control circuit for controlling a communication with said IC card. Omichi discloses sending of data blocks from the external device containing mode identification information to determine kind of processing, which constitutes controlling a communication with said IC card(see page 7).

a communication microcomputer for sending said test program to said IC card when checking the built-in nonvolatile memory therein. It would be inherent for the external device to have a communication microcomputer in order to establish a

Art Unit: 2184

communication means with the IC card, enabling it to send said test program to said IC card.

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM (see item 4 figure 1 and page 5).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5,7,12, and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Omichi in further view of US Patent No 5,818,848 of Lin et al. referred hereinafter "Lin".

In regards to claim 5 and 7, Omichi teaches all claimed subjected matter, as stated above, except a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively.

However, Lin discloses a check system comprising of a control computer connected to a plurality of integrated circuits comprising of a test circuitry, for intensively control a check-up of a plurality of integrated circuits (see figure 2 and column 2 lines 21-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Omichi and to incorporate a check system including a control computer, connected to a plurality of external communication



Art Unit: 2184

devices, for intensively controlling a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively. A person of ordinary skill in the art would have been motivated to make the modification to Omichi because Omichi discloses the testing of microcomputers and having a control computer, connected to a plurality of integrated circuits or external communication devices which are connected to a corresponding microcomputer, as per teaching of Lin, would provide for an more efficient means of testing of microcomputers.

In regards to claim 12 and 14, Omichi teaches all claimed subjected matter, as stated above, except a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively.

However, Lin discloses a check system which comprises a control computer connected to a plurality of integrated circuits comprising of a test circuitry, for intensively control a check-up of a plurality of integrated circuits (see figure 2 and column 2 lines 21-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Omichi and to incorporate a check system including a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively. A person of ordinary skill in the art would have been motivated to make the modification to Omichi because Omichi discloses the testing of an IC card and having a control computer, connected to a plurality of integrated circuits or external communication devices which are connected to a corresponding IC card, as per teaching of Lin, would provide for an more efficient means of testing of IC cards.

### ***Response to Amendment***

Art Unit: 2184

6. Applicant's arguments filed January 28, 2003 have been fully considered but they are not deemed to be persuasive.

7. In response to applicant's argument on page 7 bottom paragraph that states: "Applicants submits that Omichi does not teach or suggest at least the claimed boot ROM having the control program recited in the claim....In the claimed invention, on the other hand, the boot ROM comprises a control program that controls communications in the microcomputer....", examiner respectfully disagrees. The argument is not persuasive because applicant argues "the boot ROM comprises a control program ....", but fails to state it in the claim. Rather the applicant claims "a boot ROM in which a control program.....", which does not disclose a connection wherein the "boot ROM" comprises "control program".

In regards to applicant's argument on page 9 top paragraph that states: "Applicants submit that Lin does not teach a plurality of external communication devices for controlling the plurality of microcomputers. Rather, the processing load of controlling the testing of integrated circuits 00,01,10, 11, 20 etc is on the test control processor 100", examiner respectfully disagrees. The argument is not persuasive because it states in the specification "the check system is arranged in such a manner that a plurality of external communication devices are controlled intensively by the control computer"(see page 14 top paragraph and figure 4), indicating the *control computer is used for intensively controlling* a check-up of a plurality of microcomputers, as cited in the claim.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

Art Unit: 2184

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Emerson Puente, whose telephone number is (703) 305-8012. The examiner can normally be reached on Monday-Friday from 8:00AM- 5:00PM, first Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Robert Beausoliel*, can be reached on (703) 305-9713 or via e-mail addressed to [*robert.beausoliel@uspto.gov*]. The fax number for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**emerson.puente@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 305-3900.

*Emerson Puente*  
5/23/03

  
ROBERT BEAUSOLIEL  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100